REMARKS

Claims 1-12, 22 and 24-25 are pending in this application. By this Amendment, claims 1-5 and 10 are amended and withdrawn claims 13-21 and 23 are cancelled without waiver or disclaimer of the cancelled subject matter. Applicant reserves the right to file a divisional application directed to the cancelled subject matter. No new matter is added.

I. Claim Rejection

The Office Action rejects claims 1-12, 22 and 24-25 under 35 U.S.C. §102(e) over U.S. Patent No. 6,501,466 to Yamagishi et al. (Yamagishi). Applicant respectfully traverses the rejection.

Regarding independent claims 1-5, 10-12 and 25, Yamagishi fails to disclose (1) a second transistor that controls an electrical connection between (and/or is coupled to) the drain and the gate (or second terminal and first control terminal) of the first transistor (claims 1-2, 4-5, 10-12 and 25), (2) "the [one] first power source line being electrically disconnected from a driving potential during at least a portion of a first period" (claims 1, 10-12 and 25), (3) "a control circuit that sets the potential of the first power source line to a plurality of potential levels or controls an electrical connection between a driving voltage and the first power source line" (claims 4-5) or "a potential of the first power source line being set to a plurality of potential levels or an electrical connection between the first power source line and a driving voltage being controlled" (claim 3); and (4) "a potential of the first power source line being set to a first voltage during at least a part of the first period" and "... being set to a second voltage that is different from the first voltage during at least a part of the second period" (claim 2).

Yamagishi discloses a drive circuit for matrix displays that includes drive thin film transistor TFT2 connected to Vdd and light emitting device OLED. The gate of transistor TFT2 is connected to the gate of conversion thin film transistor TFT1. Data line DATA,

having current source CS, is connected by input thin film transistor TFT3 to the drain of transistor TFT1. Switch thin film transistor TFT4 is connected across the drain and gate of transistor TFT1. Yamagishi does not disclose that Vdd is variable, controlled, or set to multiple potential levels. Further, Yamagishi fails to disclose that there is a period in which the power source line Vdd is electrically disconnected from a driving potential to which a source or drain of a transistor is electrically connected during another period.

Regarding feature (1) above, Yamagishi fails to disclose this feature because TFT4, alleged by the Office Action as corresponding to the recited second transistor of claims 1-2, 4-5, 10-12 and 25, does not control the connection between the drain and gate of TFT2, alleged by the Office Action as corresponding to the recited first transistor. Yamagishi fails to disclose features (2)-(4) above because Yamagishi does not disclose that Vdd is ever at a potential other than a continuous, constant potential.

For the foregoing reasons, Applicant requests withdrawal of the rejection.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jonathan H. Backenstose
Registration No. 47,399

JAO:JHB/ccs

Attachment:
Request for Continued Examination

Date: June 12, 2007

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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